IN THE CLAIMS

1-8 (Cancelled)

9. (Currently amended) A method of manufacturing a non-volatile memory device, the method comprising:

forming gate stack structures on a semiconductor substrate, the gate stack structures separated by a first space on a first area of the substrate and by a second space, wider than the first space, on a second area of the substrate adjacent to the first area;

forming first gate spacers on sidewalls of the gate stack structures, the first gate spacers comprising an insulating material having a relatively low dielectric constant; ~~and~~

forming second gate spacers on the first spacers to fill the first space, the second gate spacers comprising an insulating material having a relatively high dielectric constant; and[[.]]

etching the second gate spacers until a surface of the gate stack structures is exposed.

10. (Original) The method as claimed in claim 9, wherein the first gate spacers comprise an oxide and the second gate spacers comprise a nitride.

11. (Original) The method as claimed in claim 9, wherein the first gate spacers are formed to have a thickness sufficient to form a gap within the first space.

12. (Original) The method as claimed in claim 11, wherein the first gate spacers are formed to have a thickness of about 500 Å.

13. (Original) The method as claimed in claim 9, wherein the second gate spacers are thinner than the first gate spacers.

14. (Original) The method as claimed in claim 9, wherein the first gate spacers are formed at a low pressure of about 0.4Torr or less so as to improve the step coverage.

15. (Original) The method as claimed in claim 9, wherein forming the first gate spacers comprises:

depositing a first insulating layer for the first gate spacer on the substrate and the gate stack structures;

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anisotropically etching the first insulating layer to form first insulating layer spacers on the sidewalls of the gate stack structures;

depositing a second insulating layer for the first gate spacer at a pressure of about 0.4 Torr or less on the substrate, the first insulating spacers and the gate stack structures; and

anisotropically etching the second insulating layer to form second insulating layer spacers on the first insulating layer spacers.

16. (Original) The method as claimed in claim 9, wherein the gate stack structure is formed by sequentially stacking a tunnel dielectric layer, a floating gate, an integrate dielectric layer and a control gate.

17. (Original) The method as claimed in claim 16, wherein the control gate comprises a polysilicon layer and a metal silicide layer formed on the polysilicon layer by a silicidation reaction.

18. (Original) The method as claimed in claim 17, wherein the metal silicide layer comprises one selected from the group consisting of cobalt silicide ($CoSi_2$), titanium silicide ($TiSi_2$) and nickel silicide ($NiSi_2$).

19. (Cancelled)

20. (Currently amended) A method of manufacturing a non-volatile memory device, the method comprising:

forming a plurality of gate stack structures on a semiconductor substrate, the gate stack structures separated by a first space on a first area of the substrate and by a second space, wider than the first space, on a second area of the substrate adjacent to the first area;

forming first gate spacers on sidewalls of the gate stack structures, the first gate spacers comprising an insulating material having a first dielectric constant; ~~and~~

forming second gate spacers on the first spacers to fill the first space, the second gate spacers comprising an insulating material having a second dielectric constant substantially higher than the first dielectric constant; and[[.]]

etching the second gate spacers until a surface of the gate stack structures is exposed.

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